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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/798,227	02/11/1997	BRENT KEETH	660073.587	2230

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EXAMINER	
PEIKARI, BEHZAD	

ART UNIT	PAPER NUMBER
2186	32

DATE MAILED: 02/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/798,227	KEETH, BRENT	
	Examiner	Art Unit	
	B. James Peikari	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *29,31* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The previous rejections based on Pricer, U.S. 5,673,005, is withdrawn due to applicants comments attached to the amendment filed on December 4, 2003, specifically page16, line 21 to page 17, line 2.

2. The previous rejections based on Shimizu et al., U.S. 5,229,929, is withdrawn due to applicants comments attached to the amendment filed on December 4, 2003, specifically page 13, lines 4-11, and page 16, line 21 to page 17, line 2.

3. The previous rejections based on Hopkins, U.S. 5,182,524, is withdrawn due to applicants comments attached to the amendment filed on December 4, 2003, specifically page16, line 21 to page 17, line 2.

4. The previous rejections based on Girmay, U.S. 5,130,565, is withdrawn due to applicants comments attached to the amendment filed on December 4, 2003, specifically page 13, lines 22-27, and page 16, line 21 to page 17, line 2.

Note: Upon careful review of the application papers and the prosecution history, it became apparent that the heretofore elusive "echo clock signal" was nothing more than a system clock signal, as output by a memory device as a feedback to a controller,

which signal had been modified by the skews and phase shifts and delays which inevitably accompany transmission of signals over bus lines and through the elements of a data processing system.

With this in mind, it became evident that the "echo clock signal" was simply a fundamental feedback signal used to continuously correct the timing errors in memory system by sending the feedback (echo) clock signal from the memory device to the memory controller, for comparison with a master clock signal, to identify any difference between the two and to produce a corrected (revised) timing signal.

This is not an oversimplification of the claims – with this understanding of "echo clock signal", the claims are quite broad, to the extent that they would have been taught by a number of prior art systems, only some of which are recited below.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over either one of Stephens, Jr. et al., U.S. 5,550,783, or Furuhata et al., U.S. 4,746,996.

(1) Stephens, Jr. et al. teach the use of an input master clock signal (the "external clock signal" a.k.a. CLK_{SYS}) and a delayed clock signal which is a modified version of the master clock signal (the "delayed internal clock signal") and a comparator

(138) to compare the two and to provide a feedback (via the "feedback circuit") from a memory device of SRAM (110) to its controller (122).

Stephens, Jr. et al. do not specifically mention the "echo clock signal" *by name*, however it would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that the "delayed internal clock signal" of Stephens, Jr. et al. is identical to the "echo clock signal" of the present claims, since both are generated to provide continuous feedback for error detection and subsequent correction in a memory system.

(2) Furuhata et al. teach the use of an input master clock signal (note the frequency of the "reference clock", f_0.) and a delayed clock signal which is a modified version of the master clock signal (actually, two frequency-divided signals input to comparator 410) and a comparator (410) to compare the two and to provide a feedback (i.e., the amount of the difference) from the memory (2) to its controllers (500 and 600) via compensation circuit 412, which provides continuous correction.

Furuhata et al. do not specifically mention the "echo clock signal" *by name*, however it would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that the "delayed internal clock signal" of Furuhata et al. is identical to the "echo clock signal" of the present claims, since both are generated to provide continuous feedback for error detection and subsequent correction in a memory system.

Response to Request for Reconsideration

7. With regard to the amendment filed on December 4, 2003, and the attached comments, these have been carefully considered, but are not deemed to put the application in condition for allowance.

(a) Four of the previously cited prior art rejections have been withdrawn for the reasons described above.

(b) As for applicant's comments regarding Stephens, Jr. et al., the argument that the patent teaches "the entire loop, including the feedback path for the loop, is contained within a single memory device". This is not convincing for at least two reasons. First, and most importantly, there is nothing in the claims to the contrary. Second, the "memory device" (SRAM 110) of Stephens, Jr. et al. is actually an entire module containing buffers, I/O, comparison logic, busses, synchronous random access memory array(s) (not shown), decoders, counters, etc and a memory controller. The adaptive feedback mechanism occurs between the memory arrays and the controller in exactly the same manner as in the claims.

(c) As for applicant's comments regarding Furuhata et al., the statement beginning on the last line of page 13, "As the Examiner recognizes, the Furuhata *et al.* patent does not disclose a memory controller that senses a timing error of a digital signal generated by a memory device", has absolutely no basis. The examiner never said or suggested those words.

In fact, the previous Office action stated that the only thing missing from the Furuhata et al. system was the *name* "echo clock signal". The claimed signal was

explicitly taught by Furuhata et al., however it was called a "delayed internal clock signal" instead of being called an "echo clock signal". That is the only difference.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (703) 305-3824.

The examiner generally works Mondays through Thursdays between 8:00 am and 9:00 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239 (Official communications)

or:

(703) 746-7240 (for Informal or Draft communications)

or:

(703) 746-7238 (for After-Final communications)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

B. James Peikari
Primary Examiner
Art Unit 2186

February 22, 2004